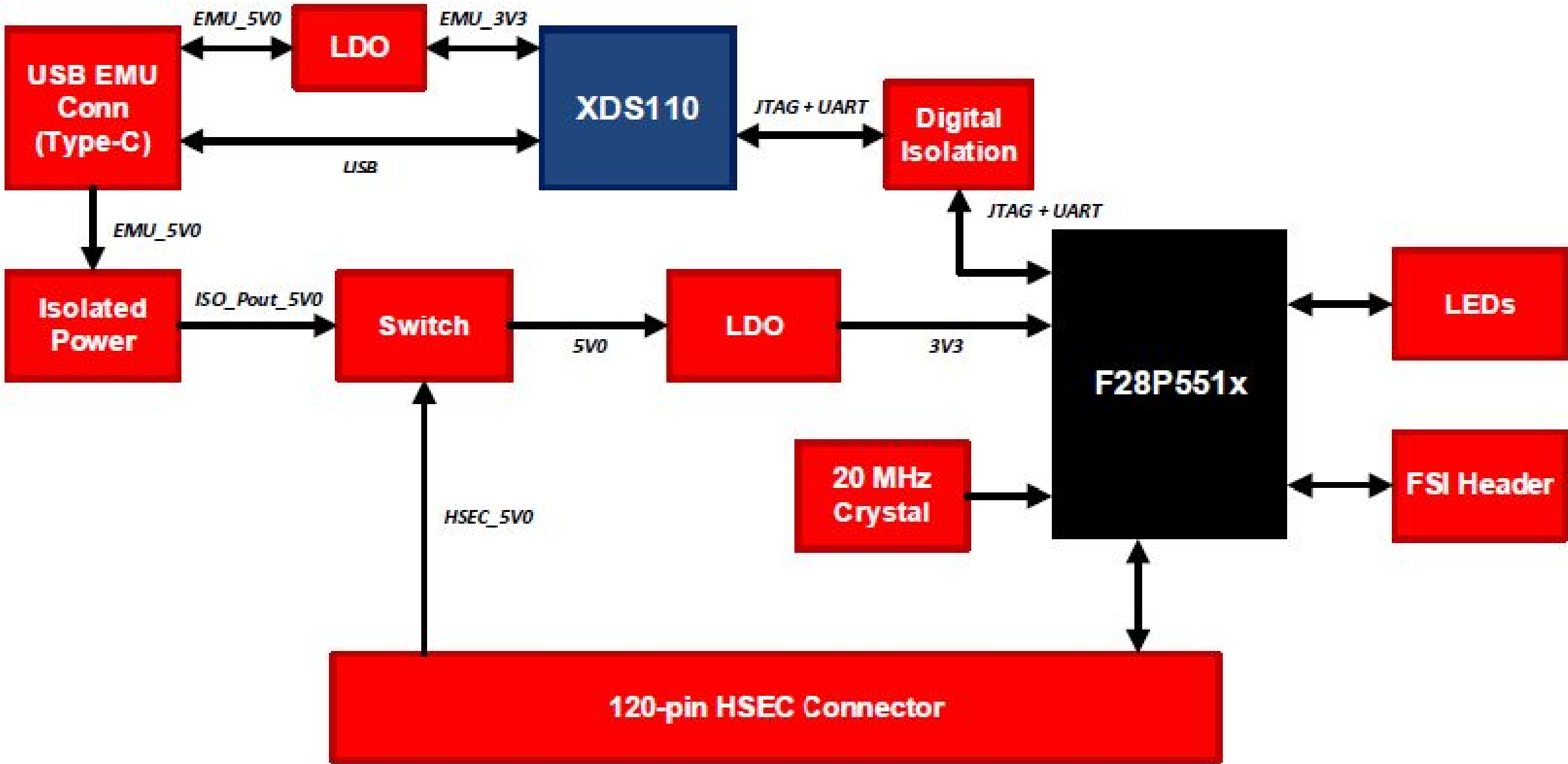
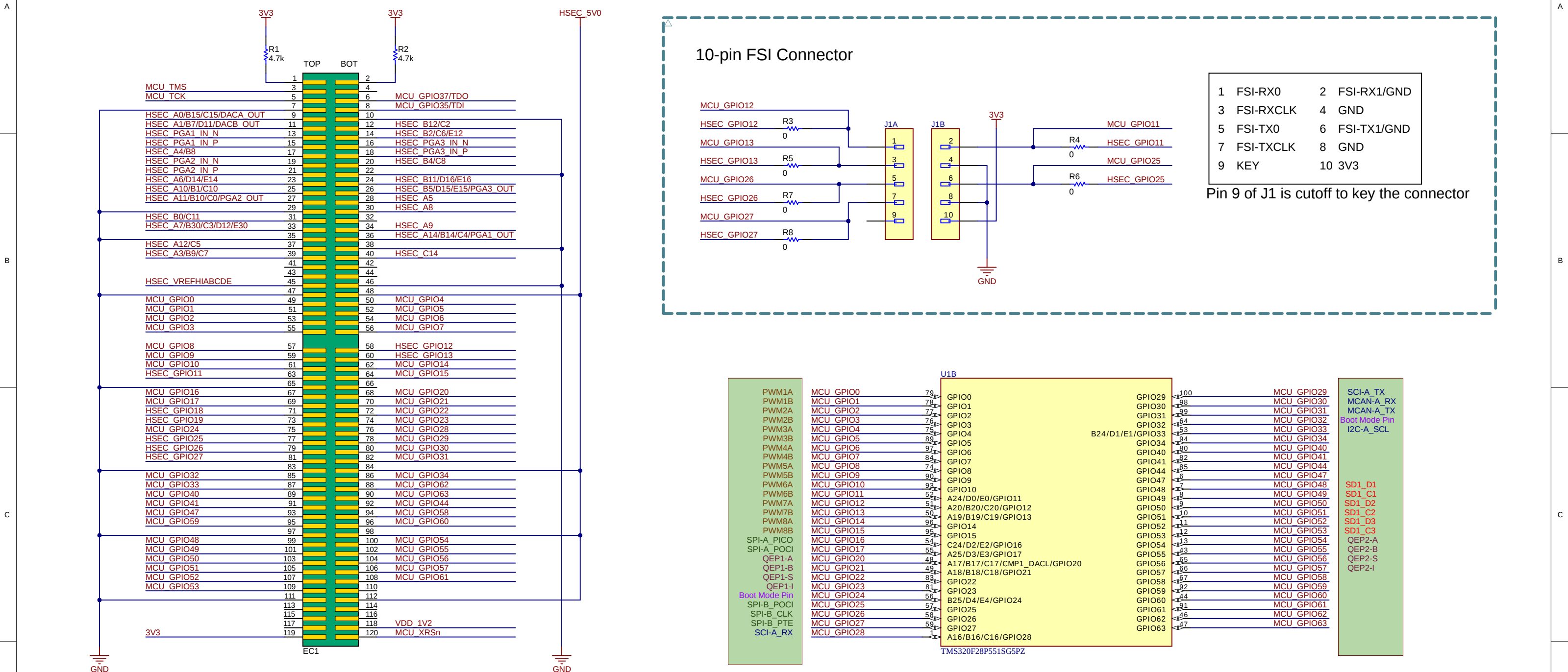


Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
A	N/A	6/4/2026	SD	Revision A



Power to the MCU is either supported by the USB-C on the left or through the HSEC

J1 has been updated over previous designs. Pins 9 and 10 were added enabling power to the connector. Additionally Pins 2 and 6, previously GND, have been repurposed to enable the full 3 pin FSI communication. The user can shunt HSEC GPIO11 and HSEC GPIO25 to ground if backwards compatibility is required.

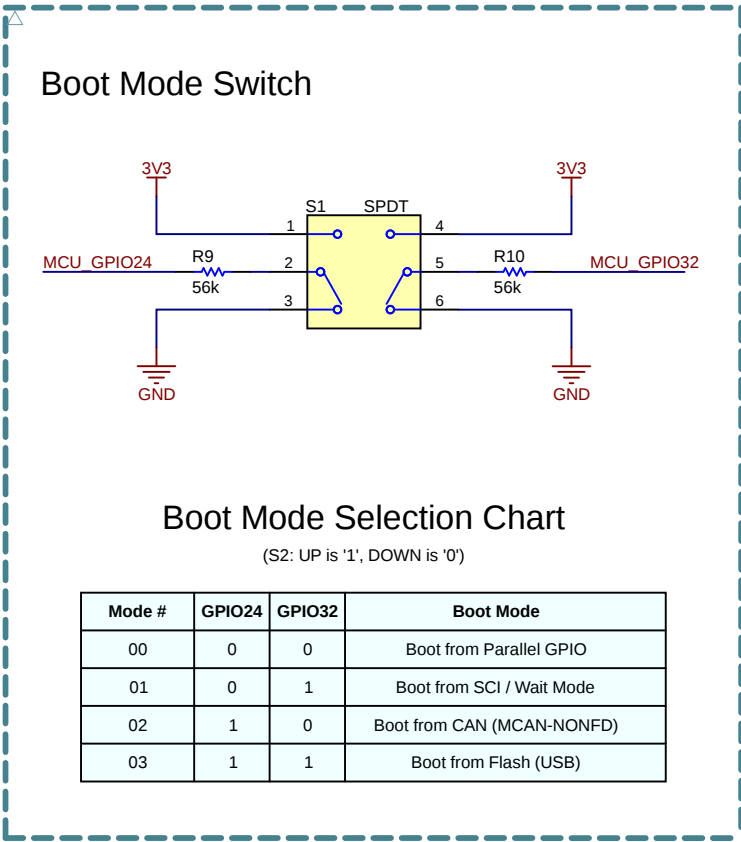
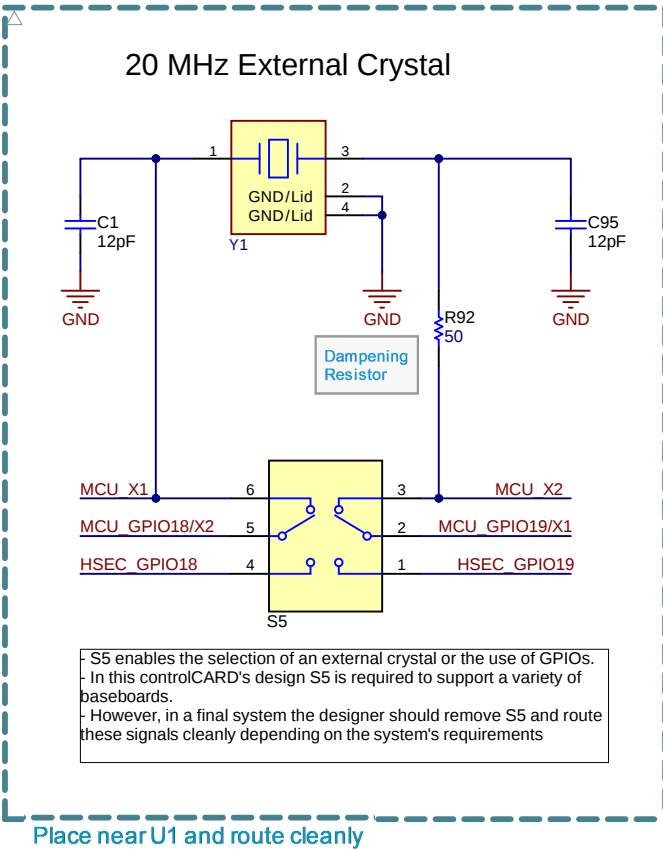
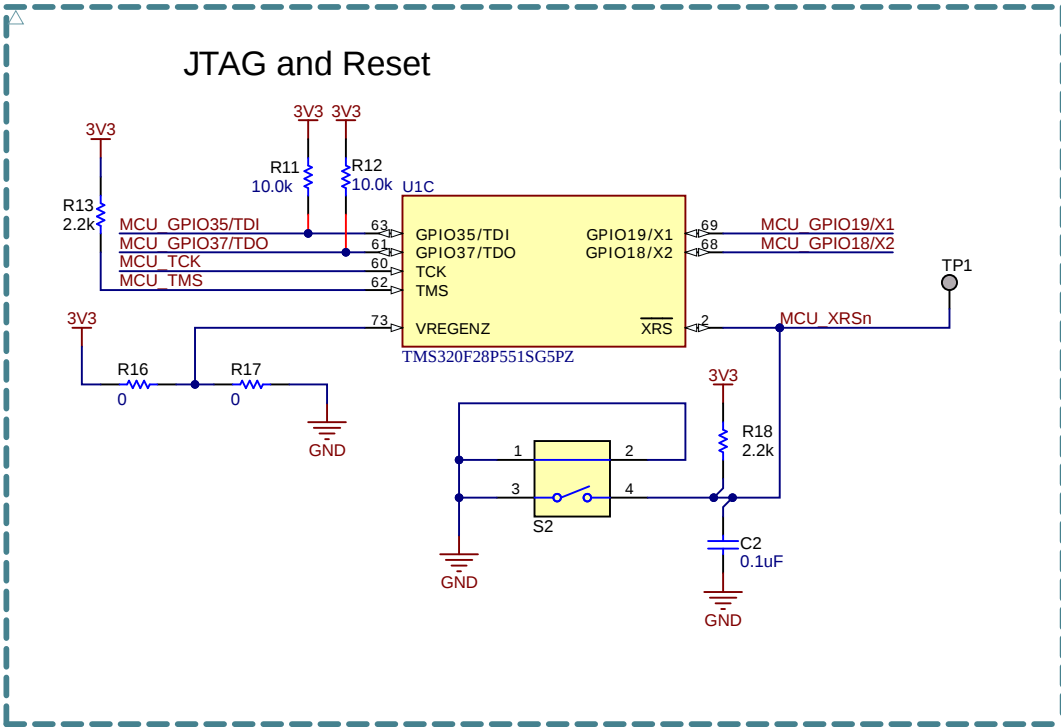


A

B

A

B

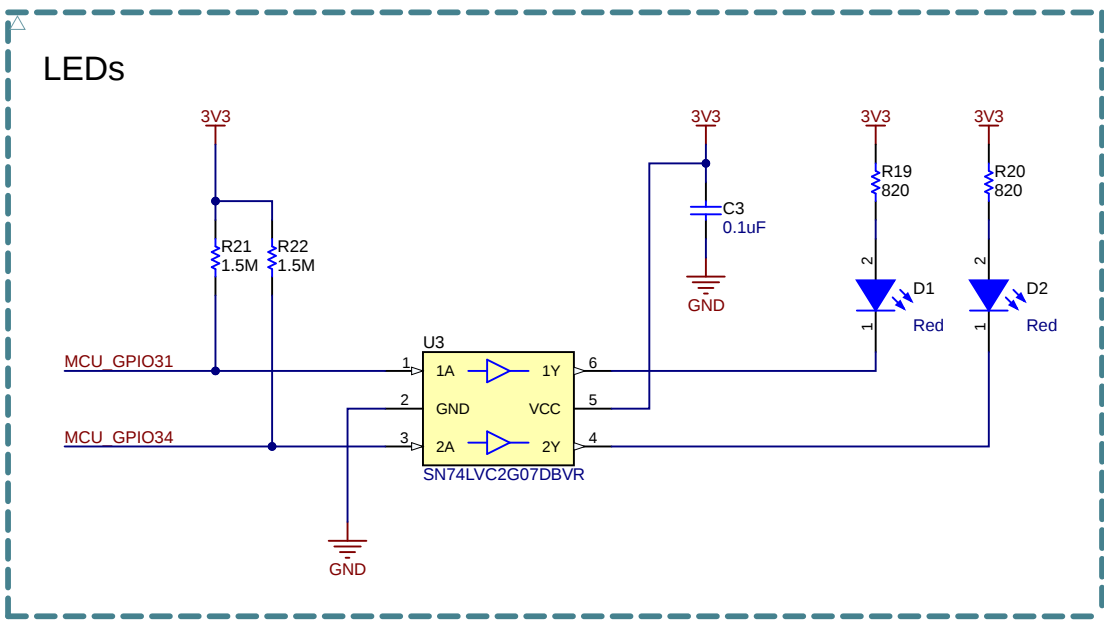
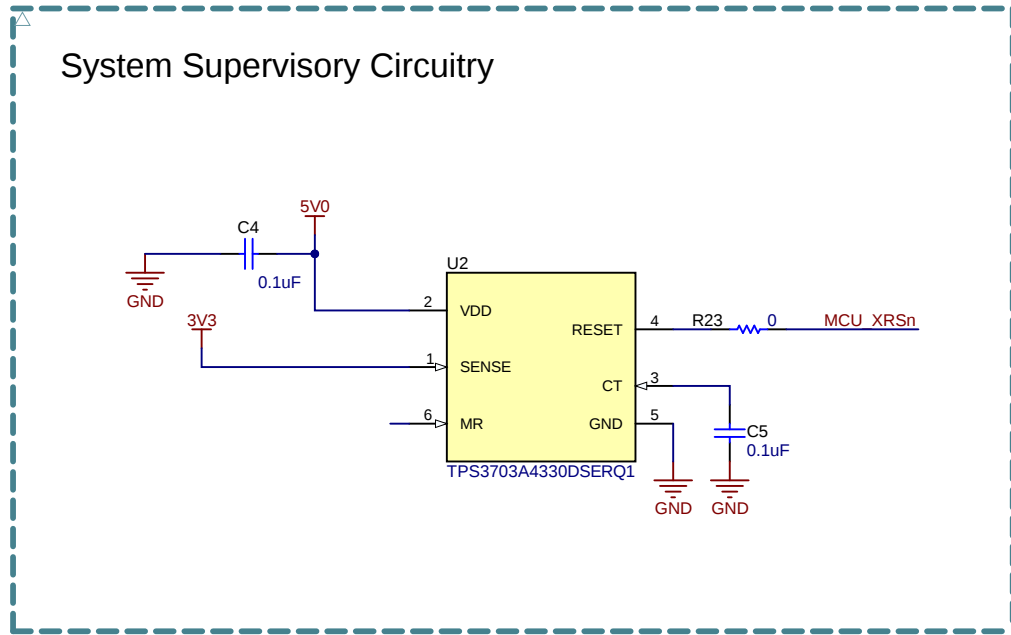


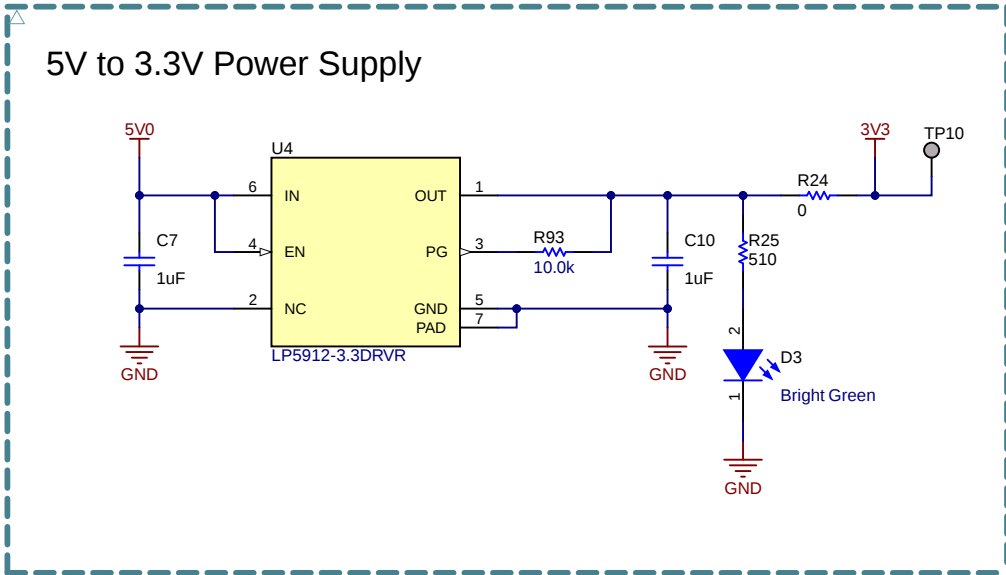
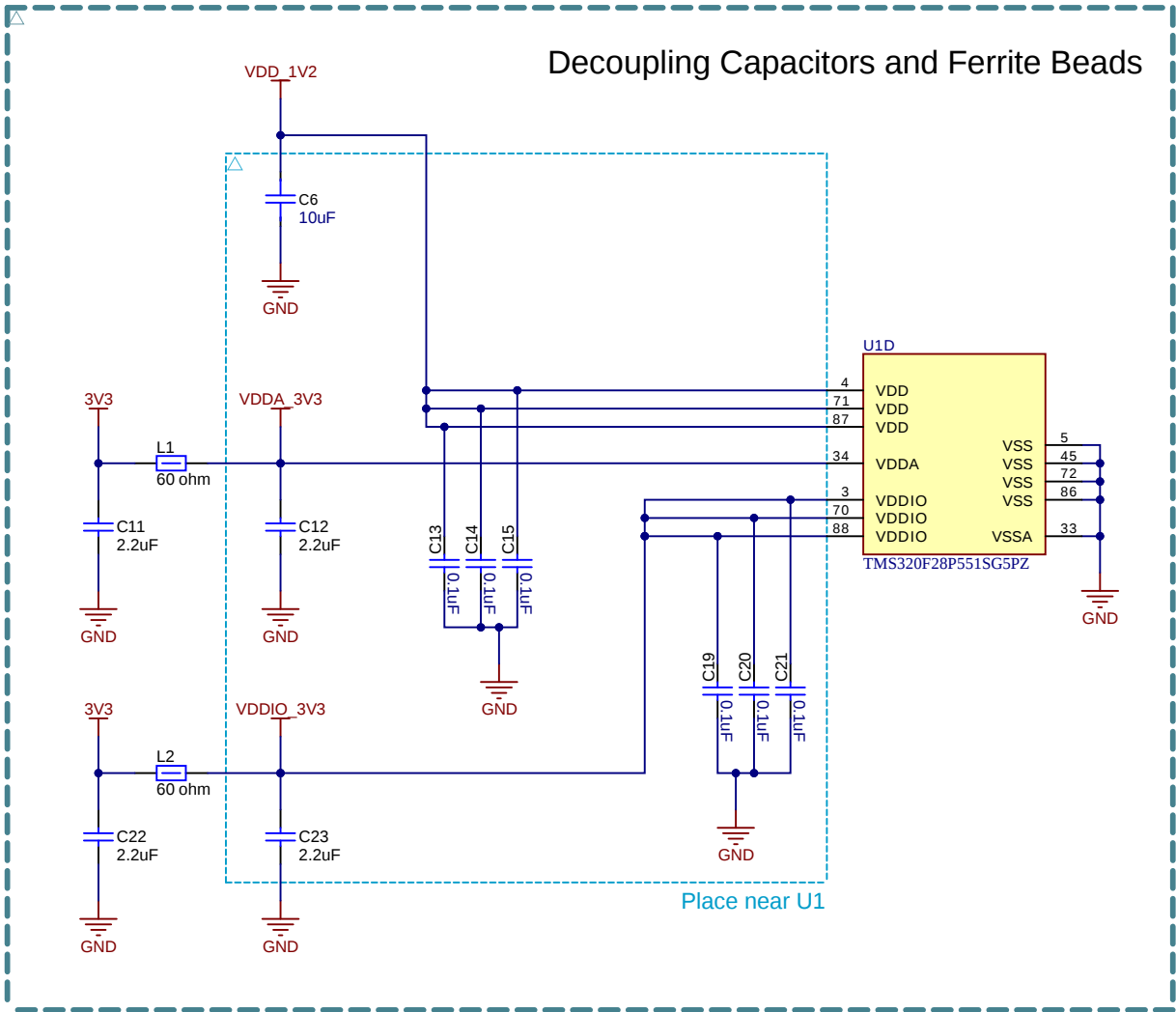
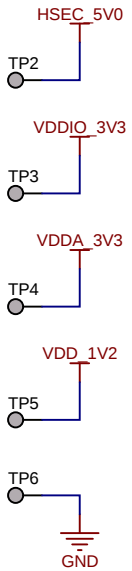
C

C

D

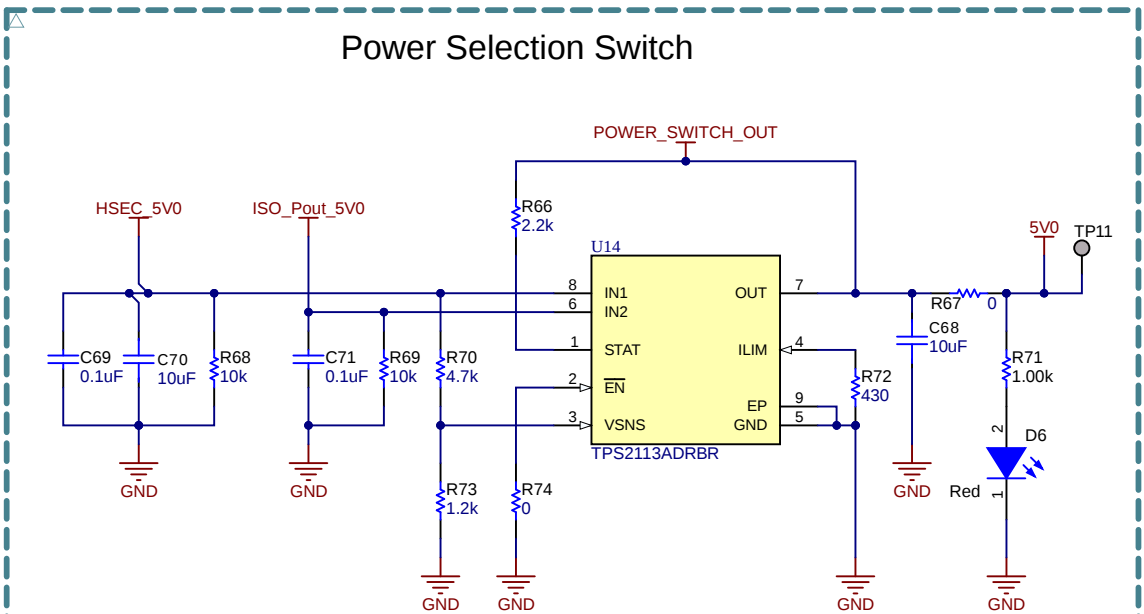
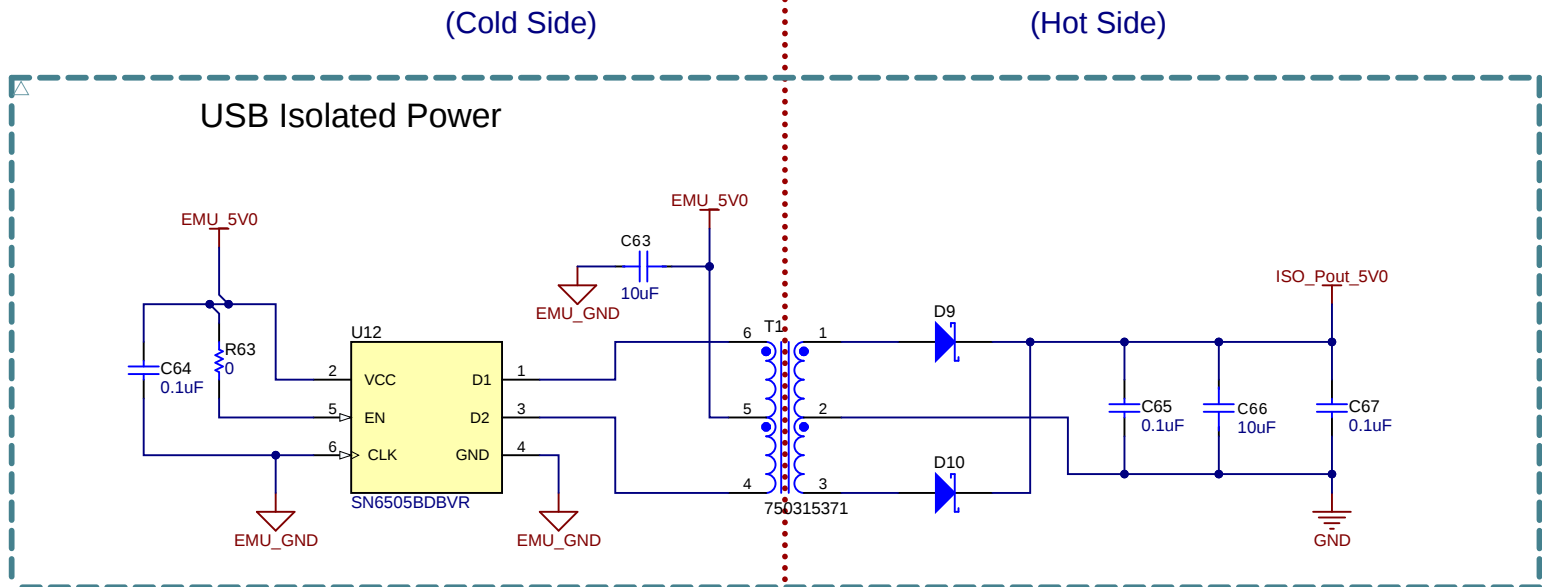
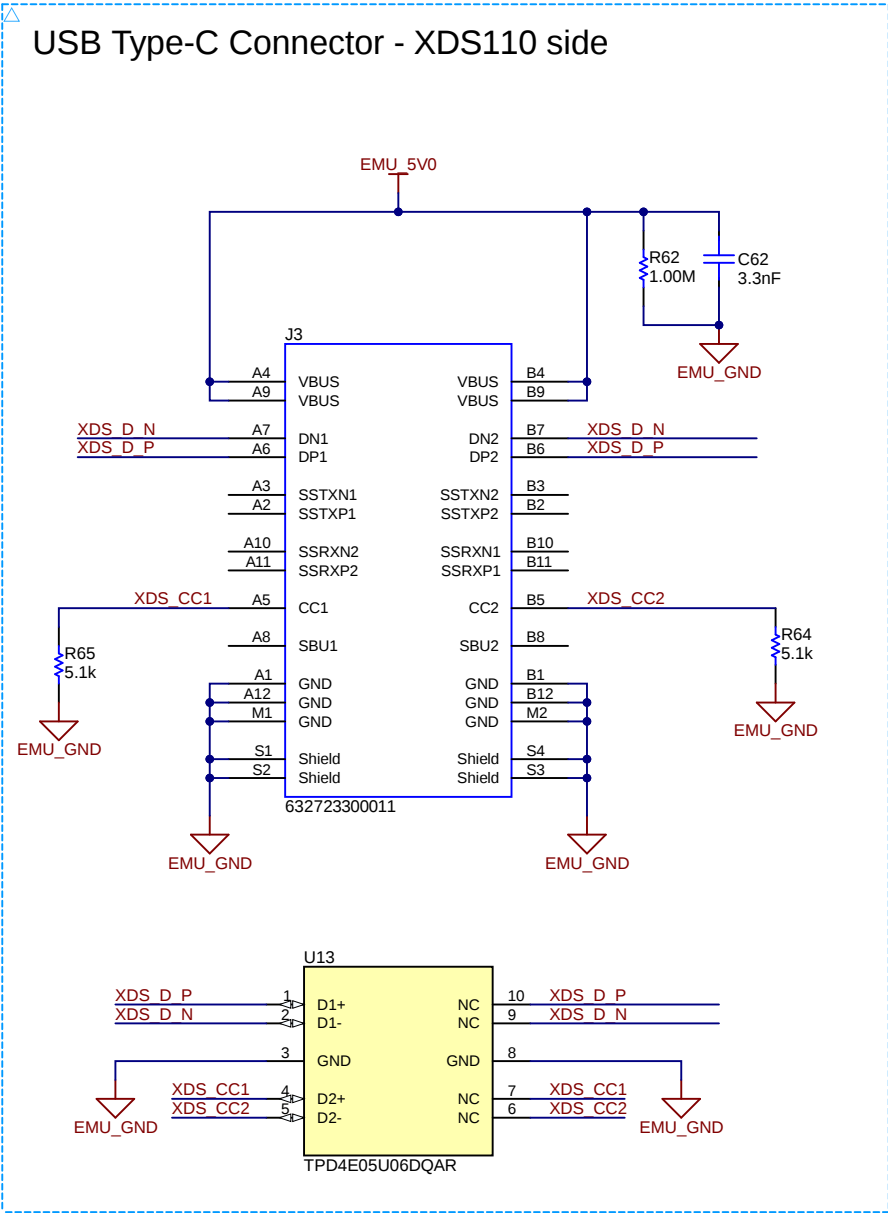
D



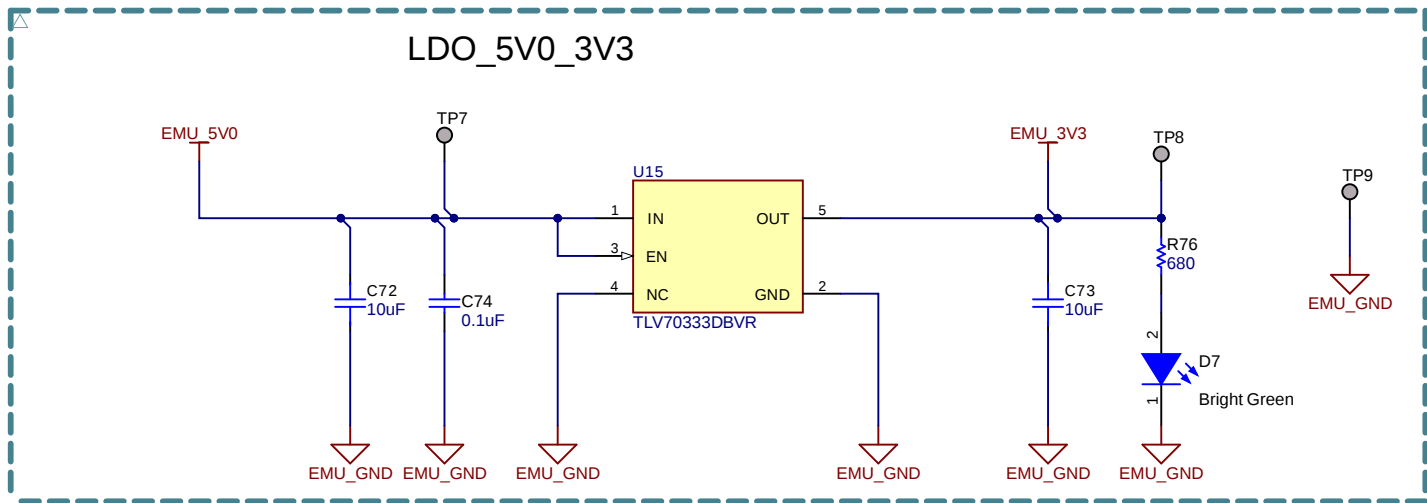


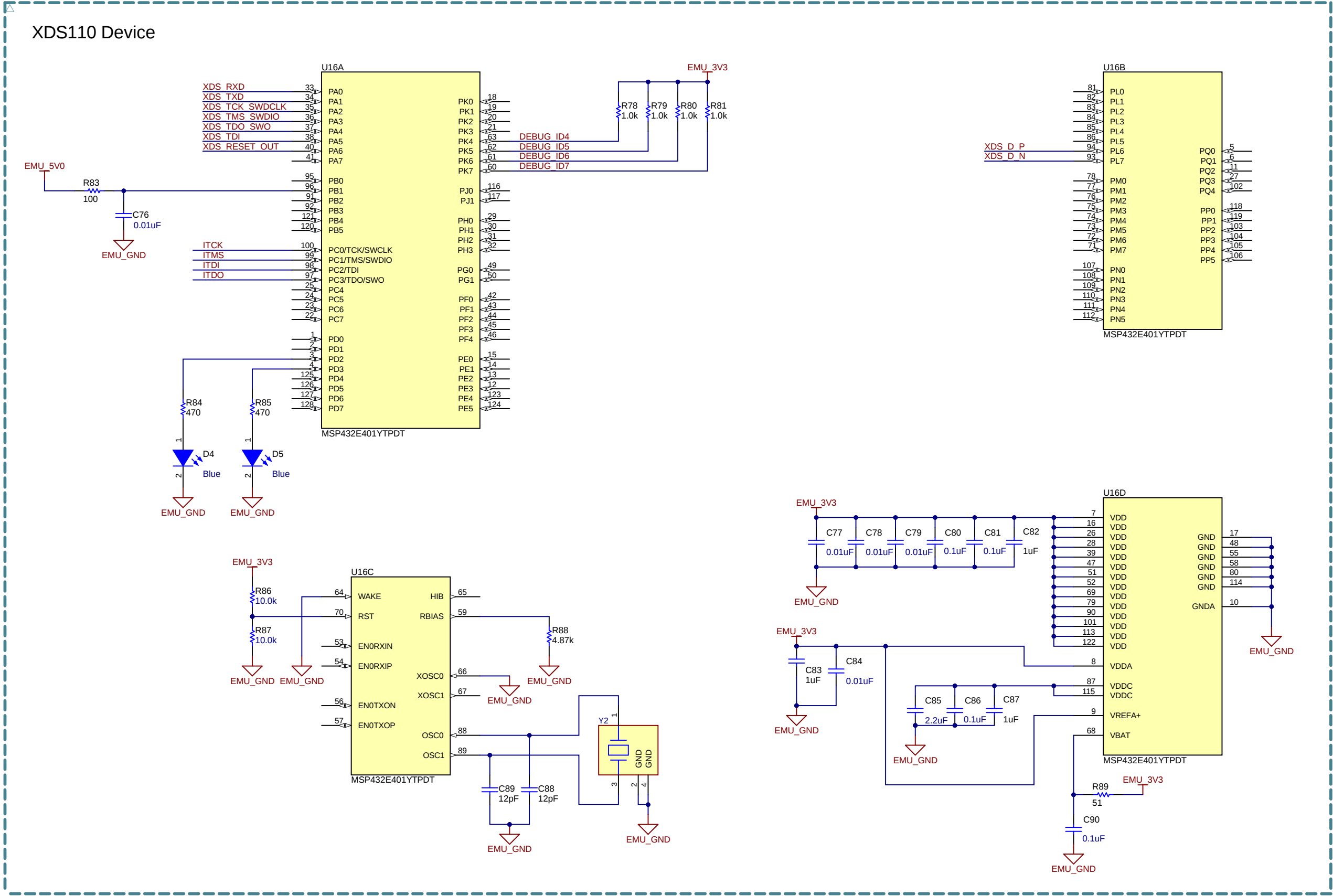
The F28P551x controlCARD uses the internal VREG to generate the 1.25V voltage rail for VDD.

For custom boards using external VREG mode, recommend to use LDO (e.g., TPS745-Q1) to generate both 3.3V and 1.25V supplies.



Switch Truth Table		
HSEC_5V0 > 4V	ISO_Pout_5V0 > HSEC_5V0	POWER_SWITCH_OUT
Yes	X	HSEC_5V0
No	No	HSEC_5V0
No	Yes	ISO_Pout_5V0





Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Orderable: TMDSCNCD28P551X	Designed for: Public Release	Mod. Date: 6/25/2025
TID #: N/A	Project Title: F28P551x controlCARD	
Number: MCU165	Rev: A	Sheet Title:
SVN Rev:	Assembly Variant: F28P551x-Required-Circuitry	Doc# 8 of 10
Drawn By: Stevan Duraskovic	File: MCU165A_XDS110_MCU.SchDoc	Size: B
Engineer: Stevan Duraskovic	Contact: http://www.ti.com/support	

A

B

C

D

A

B

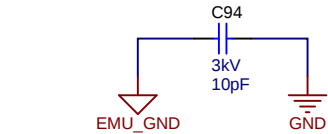
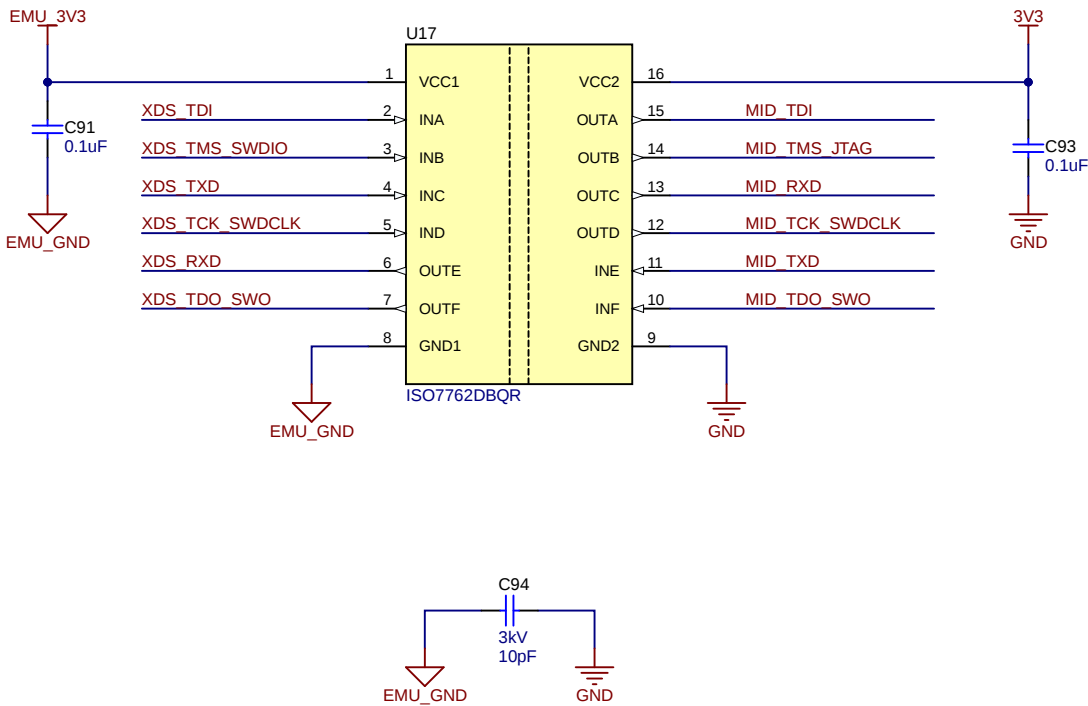
C

D

NOTE: Because the JTAG signals are isolated, cJTAG is not supported on this controlCARD.

(Cold Side)

(Hot Side)



WARNING: To avoid potential shock hazard in high-voltage settings, leave the Y cap (C94) unpopulated from the EVM.

S4 - JTAG Emulation & UART Switch

POS 1 ON: Use XDS110 emulator that is on the cCARD
POS 1 OFF: Boot from FLASH/peripheral (see boot mode switch) OR use emulator on baseboard
POS 2 ON: GPIOs 28 & 29 will be connected to the USB-to-UART adapter on the XDS110 emulator
POS 2 OFF: GPIOs 28 & 29 are disconnected from the USB-to-UART adapter on the XDS110 emulator and connected to the HSEC connector pins

